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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/030,435	01/10/2002	Takashi Kariya	217883US3PCT	6548

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EXAMINER	
GOFF II, JOHN L	

ART UNIT	PAPER NUMBER
1733	

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/030,435	KARIYA, TAKASHI	
	Examiner	Art Unit	
	John L. Goff	1733	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment received 2/23/04. The previous objections to the claims and specification have been overcome.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Specification

3. The substitute specification submitted 2/23/04 has been entered. However, the disclosure is objected to because of the following informalities: On page 1, line 13 after "A copper foil is bonded to the insulating substrate side of the one-side copper-clad laminate by pressing" insert - - and - -.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Gerber et al. (U.S. Patent 5,401,913).

Gerber et al. disclose a method for manufacturing a multilayer circuit board. Gerber et al. teach forming a single circuit board by providing an insulating layer (e.g. 10 of Figure 8), forming a conductor layer on one side of the insulating layer (e.g. 12, 16, and 22 of Figure 8), forming a via hole (e.g. 18 of Figure 5) through the insulating layer to the conductor layer, filling at least part of the via hole with a first conductor material (e.g. 20 of Figure 8) wherein at least part of the upper surface of the conductor material is lower than the upper surface of the insulating substrate, and then forming a conductive bump (e.g. 22 of Figure 8) on the first conductor material from a second conductive material having a low melting point such that the bump projects from the upper surface of the insulating substrate (Figures 1-8 and Column 3, line 1 and Column 4, lines 1, 9-12, 42-43, and 63-68 and Column 5, lines 1-5 and 15-21). Gerber et al. teach manufacturing the multilayer circuit board by applying heat and pressure to a multilayer stack comprising a plurality of single circuit board layers (as described above) having a first (i.e. upper) outermost conductor layer (e.g. a copper substrate as disclosed in Column 6, lines 1-3 and Column 7, lines 18-28) and a second (i.e. lower) outermost conductor layer (e.g. 34 and 50 of Figure 9 wherein the conductor layer has a uniform thickness throughout) with a layer of adhesive (e.g. 24 of Figure 9) interposed between each layer in the stack such that the layers of the stack are bonded to form a multilayer circuit board with the conductive bump of each circuit board connected to the conductor layer of an adjacent circuit board (Figures 9 and 10 and Column 5, lines 46-55 and 61-68 and Column 6, lines 1-3 and 12-21 and Column 7, lines 18-28).

Claim Rejections - 35 USC § 103

6. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gerber et al. in view of either one of Bohn (U.S. Patent 6,537,412) or Johnston (U.S. Patent 5,153,050).

Gerber et al. is described in full detail above. As noted above, Gerber et al. teach the plurality of single circuit board layers are bonded to an outermost conductor layer, this feature being disclosed by way of example in Gerber et al. (See Column 6, lines 1-3 and Column 7, lines 18-28). In the event this is not seen as an explicit teaching of an outermost conductor layer the following rejection is set forth. It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the outermost insulating layer of the multilayer stack taught by Gerber et al. (e.g. 32 of Figure 10) to a conductor substrate during the heat and pressing step through a layer of adhesive as was well known and conventional in the art as shown for example by either one of Bohn or Johnston to form a multilayer circuit board that is operational.

Bohn and Johnston both disclose the well known and conventional method for forming a multilayer printed circuit board by providing a stack of printed boards layers, i.e. insulating layers having conductors thereon, placing outermost conductor layers on the stack, interposing adhesive layers between all of the individual layers, and laminating the stack (Figure 1 and Column 1, lines 27-28 and Column 3, lines 49-58 of Bohn and Figure 1 and Column 1, lines 11-19 and Column 4, lines 23-57 of Johnston). Bohn additionally teaches that in forming a multilayer circuit board the internal circuit board structures may be any that are desired it being only essential that the outer sides are covered by conductor layers (Column 1, lines 27-28 and Column 3, lines 56-58).

Response to Arguments

7. Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection. Applicant argues, "It is clear from the above-noted summary of Johnston that this prior art reference cannot obviate a method in which each printed board has a via hole extending through the insulating substrate to the conductor layer filled with a plate conductor being formed with a conductive bump extending through the bonding layer so that the conductive bump is connected to the conductor layer of the other stacked printed board. There are at least no via holes extending through the insulating substrate to the conductor layer in Johnston and Johnston is silent with respect to filling the via holes with a plate conductor formed with a conductive bump extending through the bonding layer so that the conductive bump is connected to the conductor layer of the other stacked printed board during pressing of the assembly." In view of applicants amendment to claim 1 the previous rejection over Johnston and Takahashi et al. is withdrawn and a new rejection using Gerber et al. is made above.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **John L. Goff** whose telephone number is **(571) 272-1216**. The examiner can normally be reached on M-F (7:15 AM - 3:45 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on (571) 272-1226. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John L. Goff
May 14, 2004

JEFF H. AFTERGUT
PRIMARY EXAMINER
GROUP 1300